CLAIMS

1. A memory apparatus using a memory element of variable resistance which changes between a high resistance state having a higher resistance than a resistance of a reference resistance element and a low resistance state having a lower resistance than the resistance of the reference resistance element in response to two kinds of data to be stored, the memory apparatus using a memory element of variable resistance characterized by a structure having the resistance of the reference resistor made variable.

2. A memory apparatus using a memory element of variable resistance which changes between a high resistance state having a higher resistance than a resistance of a reference resistance element and a low resistance state having a lower resistance than the resistance of the reference resistance element in response to two kinds of data to be stored, the memory apparatus using a memory element of variable resistance characterized by a structure in which a reference circuit, made of a first resistance element and the reference resistance element connected in series between reference potential terminals set to different potentials, and a memory circuit, made of a second resistance element and the memory element of changeable resistance connected in series, are connected in parallel, wherein the resistance of the reference resistance is variable.

3. A memory apparatus using a memory element of variable resistance which changes between a high resistance state having a higher resistance than a resistance of a reference resistance element and a low resistance state having a lower

resistance than the resistance of the reference resistance element in response to two kinds of data to be stored, the memory apparatus using a memory element of variable resistance characterized by a structure in which a reference circuit, made of a first resistance element and the reference resistance element connected in series between reference potential terminals set to different potentials, and a memory circuit, made of a second resistance element and a memory element of variable resistance selected from a plurality of memory elements of variable resistances connected in series, both connected in parallel, wherein the resistance of the reference resistance is variable.

4. The memory apparatus using a memory element of variable resistance as claimed in claim 2 or 3, wherein the second resistance element has a variable resistance.

5. The memory apparatus using a memory element of variable resistance as claimed in any of claims 2 to 4, wherein the first resistance element is variable so as to have a same resistance as the resistance of the second resistance element.

6. The memory apparatus using a memory element of variable resistance as claimed in any of claims 2 to 5,, wherein an electric potential on a junction between the first resistance element and the reference resistance element is a reference potential, the potential on a junction between the second resistance element and the memory element of variable resistance is a memory potential, and comparison is made between the reference potential and the memory

potential to judge that the resistance of the memory element of variable resistance is in a high resistance state if the memory potential is higher than the reference potential, while the memory element of variable resistance is in a low resistance state if the memory potential is lower than the reference potential.

7. A memory apparatus using a plurality of memory elements of variable resistance which change between a high resistance state having a higher resistance than a reference resistance and a lower resistance state having a lower resistance than the reference resistance in response to two kinds of data to be stored, wherein

the reference resistance is determined as a resistance between a lowest resistance among the memory elements of variable resistances in the high resistance state and the highest resistance in the low resistance state.

8. A reference resistance determination method for a memory apparatus using a memory element of variable resistance, comprising the steps of:

setting a lowest resistance among part of a plurality of memory elements of variable resistance in a high resistance state as a temporary reference resistance;

setting a lowest resistance among memory elements of variable resistance within the remaining memory elements of variable resistance determined as having lower resistance than the temporary reference resistance in the high resistance state as a lowest resistance in the high resistance state;

setting a highest resistance among part of the

plurality of memory elements of variable resistance in a low resistance state as a temporary reference resistance;

setting a highest resistance among memory elements of variable resistance within the remaining memory elements of variable resistance determined as having higher resistance than the temporary reference resistance in the low resistance state as a highest resistance in the low resistance state; and

determining a resistance between the lowest resistance in the high resistance state and the highest resistance in the low resistance state as the reference resistance.